WE CLAIM:

1. A bipolar differential input stage which includes an input bias current cancellation circuit, comprising:

first and second bipolar input transistors having their bases connected to first and second input terminals, respectively, and their emitters connected together at a common emitter node;

a first current source connected to said common emitter node and arranged to provide a first bias current I_{bias1} to said first and second input transistors;

a bipolar tracking transistor;

a second current source which provides a second bias current I_{bias2} to said tracking transistor;

said input stage arranged such that the collector currents in and the collector-emitter voltages of said first and second input transistors and said tracking transistor are substantially equal when the voltages at said first and second input terminals are equal; and

a base current copy circuit arranged to provide a base current I_{trk} to said tracking transistor required to achieve said substantially equal collector current in said tracking transistor, said copy circuit further arranged to provide first and second bias current cancellation currents I_{cncl1}, I_{cncl2} to the bases of said first and second input transistors, respectively, such that $I_{cncl1} \approx I_{cncl2} \approx I_{trk}$, thereby reducing the input stages' input bias currents.

2. The input stage of claim 1, wherein I_{bias2} is substantially equal to $I_{bias1}/2$.

3. The input stage of claim 1, wherein said input stage is the input stage of an operational amplifier.

4. The input stage of claim 1, wherein said input stage is the input stage of a comparator.

5. The input stage of claim 1, wherein said input stage is the input stage of an instrumentation amplifier.

6. A bipolar differential input stage which includes an input bias current cancellation circuit, comprising:

first and second bipolar input transistors (Q1,Q2) having their bases connected to first and second input terminals, respectively, and their emitters connected together at a common emitter node, said first and second transistors biased to conduct respective output currents in response to a differential input signal applied to said first and second input terminals;

first and second bipolar cascode transistors (Q4,Q5) connected in series between said a first supply voltage and said first and second input transistors, respectively, such that said first and second cascode transistors conduct said first and second output currents, the bases of said first and second cascode transistors connected together at a second node;

a bipolar tracking transistor (Q3) having its emitter connected to said common emitter node;

a first current source connected to said common emitter node and arranged to provide a first bias current I_{bias1} at said common emitter node;

a third cascode transistor (Q6) having its base connected to said second node and its collector-emitter circuit connected in series between a second current source and said tracking transistor, said second current source arranged such that said third cascode transistor and said tracking transistor conduct a current given by $I_{bias1}/3$, such that the collector currents in and the collector-emitter voltages across said first and second input transistors and

said tracking transistor are substantially equal when the voltages at said first and second input terminals are equal; and

a base current copy circuit arranged to provide a base current I_{trk} to said tracking transistor such that it conducts $I_{bias1}/3$, said copy circuit further arranged to provide first and second bias current cancellation currents I_{cncl1}, I_{cncl2} to the bases of said first and second input transistors, respectively, such that $I_{cncl1} \approx I_{cncl2} \approx I_{trk}$, thereby reducing the input stages' input bias currents.

7. The input stage of claim 6, wherein said base current copy circuit comprises a lateral PNP transistor (Q7) having first, second and third collectors, said lateral PNP transistor having its first collector connected to the base of said tracking transistor and providing I_{trk}, and its second and third collectors connected to the bases of said first and second input transistors and conducting I_{cncl1} and I_{cncl2}, respectively, wherein said input range has an associated common mode input voltage range, said lateral PNP transistor connected such that its emitter-base junction is forward-biased and its base-collector junction is reverse-biased such that said lateral PNP transistor operates in its linear region over said common mode input voltage range.

8. The input stage of claim 7, wherein said lateral PNP transistor's emitter is connected to the collector of said third cascode transistor.

9. The input stage of claim 8, further comprising:

a PNP transistor (Q8) having its base connected to said common emitter node, its collector coupled to a second supply voltage, and its emitter connected to a third node; and

a diode-connected NPN transistor (Q9) having its base/collector connected to said second node and to a current source 42 coupled to said first supply voltage, and its emitter connected to said third node;

the base of said lateral PNP transistor connected to said third node.

10. The input stage of claim 7, wherein said first current source comprises a first current source transistor (Q10) having its collector connected to said common emitter node, its emitter coupled to a second supply voltage, and its base connected to a bias voltage V_B;

said second current source comprising:

a second current source transistor (Q11) having its emitter coupled to said second supply voltage and its base connected to V_B, and first and second current sources arranged such that said second current source transistor conducts $I_{bias1}/3$; and

a current mirror (Q13/Q14) connected to mirror the current conducted by said second current source transistor to the collector of said third cascode transistor.

11. The input stage of claim 10, wherein said first current source transistor is coupled to said second supply voltage via a first resistance and said second current source transistor is coupled to said second supply voltage via a second resistance, said first resistance made equal to approximately one-third of said second resistance, and the ratio between the emitter size of said first current source transistor and the emitter size of said second current source transistor made to be approximately 3:1.

12. The input stage of claim 10, wherein said input stage provides a voltage loop between the collector of said

first current source transistor and the collector of said second current source transistor such that Early effect-induced errors that might otherwise arise when the input stage's common mode input voltage changes are reduced.

13. The input stage of claim 10, wherein said current mirror comprises a diode-connected PNP input transistor (Q13) and a PNP output transistor (Q14), the emitters of said mirror transistors connected to a fourth node via respective resistances (R4/R5), said fourth node coupled to said first supply voltage via the collector-emitter circuit of a PNP transistor (Q15) which receives a bias voltage at its base such that it provides a current approximately equal to I_{bias1} to said fourth node.

14. The input stage of claim 13, further comprising:

a PNP transistor (Q8) having its base connected to said common emitter node, its collector connected to said second supply voltage, and its emitter connected to a third node; and

a diode-connected NPN transistor (Q9) having its base/collector connected to said second node and to a resistor (R3), the other side of R3 connected to said fourth node, and its emitter connected to said third node;

said lateral PNP's base connected to said third node, and its emitter connected to the collector of said third cascode transistor;

wherein said second current source further comprises a diode-connected NPN transistor (Q12) connected between said current mirror and said second current source transistor, said input stage thereby providing a voltage loop between the collector of said first current source transistor and the collector of said second current source transistor via the base-emitter junction of Q8, the base-emitter junction of Q9, R3, R4, the base-emitter junction

of Q13, and the base-emitter junction of Q12, such that Early effect-induced errors that might otherwise arise when the input stage's common mode input voltage changes are reduced.

15. The input stage of claim 14, wherein said input stage is arranged such that $V_{be(Q8)} + V_{be(Q9)} + I*R3 = I*R4 + V_{be(Q13)} + V_{be(Q12)}$ such that the collector voltage of said first current source transistor is approximately equal to the collector voltage of said second current source transistor.

16. The input stage of claim 14, further comprising a resistor connected between the collector and base of Q13 such that Q13 overdrives mirror transistor Q14 to compensate for the emitter current of said lateral PNP transistor which is diverted from the collector of said third cascode transistor.

17. A bipolar differential input stage which includes an input bias current cancellation circuit, comprising:

first and second bipolar input transistors (Q1,Q2) having their bases connected to first and second input terminals, respectively, and their emitters connected together at a common emitter node, said first and second transistors biased to conduct respective output currents in response to a differential input signal applied to said first and second input terminals;

first and second bipolar cascode transistors (Q4,Q5) connected in series between said a first supply voltage and said first and second input transistors, respectively, such that said first and second cascode transistors conduct said first and second output currents, the bases of said first and second cascode transistors connected together at a second node;

a bipolar tracking transistor (Q3) having its emitter connected to said common emitter node;

a first current source comprising a first current source transistor (Q10) having its collector connected to said common emitter node, its emitter coupled to a second supply voltage, and its base connected to a bias voltage V_B, said first current source arranged to provide a first bias current I_{bias1} at said common emitter node;

a second current source comprising a second current source transistor (Q11) having its emitter coupled to said second supply voltage and its base connected to V_B, said first and second current sources arranged such that said second current source transistor conducts $I_{bias1}/3$;

a current mirror (Q13/Q14) connected to mirror the current conducted by said second current source transistor to a third node;

a third cascode transistor (Q6) having its base connected to said second node and its collector-emitter circuit connected in series between said third node and said tracking transistor such that said third cascode transistor and said tracking transistor conduct a current given by $I_{bias1}/3$, such that the collector currents in and the collector-emitter voltages across said first and second input transistors and said tracking transistor are substantially equal when the voltages at said first and second input terminals are equal; and

a lateral PNP transistor (Q7) having first, second and third collectors, said lateral PNP transistor having its first collector connected to the base of said tracking transistor and providing I_{trk}, and its second and third collectors connected to the bases of said first and second input transistors and conducting I_{cncl1} and I_{cncl2} to the bases of said first and second input transistors, respectively, said lateral PNP transistor biased such that its emitter-base junction is forward-biased and its base-

collector junction is reverse-biased such that said lateral PNP transistor operates in its linear region and $I_{cncl1} \approx I_{cncl2} \approx I_{trk}$, thereby reducing the input stages' input bias currents.

18. The input stage of claim 17, wherein said input stage provides a voltage loop between the collector of said first current source transistor and the collector of said second current source transistor such that Early effect-induced errors that might otherwise arise when the input common mode voltage changes are reduced.

19. The input stage of claim 18, wherein said current mirror comprises a diode-connected PNP input transistor (Q13) and a PNP output transistor (Q14), the emitters of said mirror transistors connected to a fourth node via respective resistances (R4/R5), said fourth node coupled to said first supply voltage via the collector-emitter circuit of a PNP transistor (Q15) which receives a bias voltage at its base such that it provides a current approximately equal to I_{bias1} to said fourth node, said input stage further comprising:

a PNP transistor (Q8) having its base connected to said common emitter node, its collector connected to said second supply voltage, and its emitter connected to a fifth node; and

a diode-connected NPN transistor (Q9) having its base/collector connected to said second node and to a resistor (R3), the other side of R3 connected to said fourth node, and its emitter connected to said fifth node;

said lateral PNP's base connected to said fifth node, and its emitter connected to the collector of said third cascode transistor;

wherein said second current source further comprises a diode-connected NPN transistor (Q12) connected

between said current mirror and said second current source transistor, said input stage thereby providing said voltage loop between the collector of said first current source transistor and the collector of said second current source transistor via the base-emitter junction of Q8, the base-emitter junction of Q9, R3, R4, the base-emitter junction of Q13, and the base-emitter junction of Q12, such that Early effect-induced errors that might otherwise arise when the input stage's common mode input voltage changes are reduced.

20. The input stage of claim 19, wherein said input stage is arranged such that $V_{be(Q8)} + V_{be(Q9)} + I*R3 = I*R4 + V_{be(Q13)} + V_{be(Q12)}$ such that the collector voltage of said first current source transistor is approximately equal to the collector voltage of said second current source transistor.